## REMARKS

Claims 41-52 are pending in the above-referenced application. Claims 41, 43, 45, 46 and 50-52 are amended to more distinctly claim Applicant's invention.

35 U.S.C. 112, second paragraph rejection:

Claims 43, 45-49 and 52 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 43 is amended to insert the word "layer" after the phrase "overlying metal". Thus the reference to "the overlying layer" now has a proper antecedent basis and the rejection of Claim 43 is overcome.

Claim 45 is amended to insert the limitation of "forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure having sidewalls" and make the remaining language consistent with this additional limitation. Applicant asserts that this amendment overcomes the rejection of Claim 45, as well as Claims 46-49 which depend from Claim 45.

Claim 52 is amended to delete the terms "patterned" and "oxidation barriers" and thus more distinctly claim the structures the Examiner found unclear. Applicant asserts that these amendments overcome the rejection of Claim 52.

35 U.S.C. 112, first paragraph rejection:

Claims 41, and 43-49 stand rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Specifically, the Examiner states that the phrase "forming oxidation resistant sidewall spacers" is critical and is not included in Claims 41 and 45. Applicant does not agree that this specific phrase must be included in a claim to enable Applicant's invention. Thus, Applicant respectfully asserts that amended Claim 41, which recites among other things, that "only a portion of the gate at the interface with the gate dielectric layer is oxidized" and amended Claim 45, which recites among other things, that "the sidewall spacers provide that only a portion of the gate at the interface with the first layer is oxidized" are enabled and distinctly claim embodiments of Applicant's invention without the specific language suggested by the Examiner. Thus Applicant requests reconsideration of amended Claims 41 and 45 as well as Claims 43, 44, and 46-49, which depend respectively from Claims 41 and 45, and withdrawal of the rejection.

Double Patenting rejection:

Claims 41-52 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-41 of U.S. Patent No. 5,739,066. Applicant includes a Terminal Disclaimer in compliance with 37 C.F.R. 1.321(c) filed herewith to overcome this rejection.

35 U.S.C. 102(e) rejections:

Claims 45, 46 and 49 stand rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (5,545,578). Applicant traverses.

Applicant's Claim 45 recites, among other things, "forming sidewall spacers over the conductive gate's sidewalls sufficiently to cover **all** conductive material comprising the sidewalls." (Emphasis added.) On the other hand, Park et al. teach forming sidewall spacers that cover only a portion of the sidewalls of the conductive material. Referring to Fig. 4E and the text describing that figure at Column 4, lines 58-64, Park et al. describe that oxidation-prevention layer 22 is anisotropically etched to form an oxidation-prevention spacer 22a that covers only the sidewalls of an upper portion of the doped polysilicon layer 14 exposed by step "a".

M.P.E.P. 706.02 states that "for anticipation under U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly." Since Park et al. do not teach that all of the conductive gate's sidewalls are covered by the sidewall spacers, as recited in Applicant's Claim 45, Applicant respectfully submits that this rejection is improper and must be withdrawn. As Claims 46 and 49 depend directly from Claim 45, they too cannot be anticipated by Park et al. and Applicant asserts that the rejection of these additional claims must also be withdrawn. Action to this end is requested.

Claims 41, 45 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (4,786,609). Applicant traverses.

Applicant's Claim 41 recites, among other things, that "**only a portion of the gate at the interface with the gate dielectric layer is oxidized**." And Applicant's Claim 45 recites, among other things, "conducting an oxidizing step by channeling oxidants through the first layer ... wherein the sidewall spacers provide that **only a portion of the gate at the interface with the first layer is oxidized**." (Emphasis added to both.) On the other hand, Chen teaches that the thickness of oxide spacers 34 is increased by oxidizing the sidewalls of the doped polysilicon layer 20A. (Col. 5, lines 3-5) And in stark contrast to Applicant's invention, as claimed, Chen describes that "[t]he amount of additional spacer thickness achieved ... is greater at the top of each spacer 34 than at the bottom." (*Ibid.*, lines 28-30).

Thus Chen does not teach the limited oxidation recited in each of Applicant's Claims 41 and 45 therefore failing to meet the requirement of anticipation as stated in M.P.E.P. 706.02. Hence, Applicant respectfully submits that this rejection is improper and must be withdrawn. As Claim 46 depends directly from Claim 45, it too cannot be anticipated by Chen and Applicant asserts that the rejection of Claim 46 must also be withdrawn. Action to this end is requested.

Claims 41-42, 45-46 and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama (JP 64 73772). Applicant traverses.

Applicant's Claim 41 recites, among other things, "exposing the substrate to **oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers** joined

therewith wherein **only a portion of the gate at the interface with the gate dielectric layer is oxidized**." (Emphasis added).

Applicant's Claim 45 recites, among other things, that "the sidewall spacers provide that **only a portion of the gate at the interface with the first layer is oxidized**." (Emphasis added).

Applicant's Claim 50 recites, among other things, "exposing the substrate to oxidizing conditions effective to oxidize **only that portion of the gate proximate the spacers and the dielectric layer**." (Emphasis added).

In Koyama, a first oxidation process is used to form thick $SiO_2$ layer 11 which is then covered by a layer 12 of $SiN_4$ which in turn is formed into what appears to be sidewall spacers 12a. Applicant asserts that it is clear from the comparison of Figs. 1c to 1d (or Figs. 3c to 3d) that the wet oxidation employed to form $SiO_2$ layer 7 increases the thickness of film 11 along the entirety of the sidewalls of doped polysilicon film 4. Hence, Koyama does not teach oxidizing conditions that oxidize only the portion of the gate at the interface with the gate dielectric layer as recited in Applicant's Claims 41, 45 and 50. Applicant respectfully submits, therefore, that Koyama does not meet the requirement of anticipation stated in M.P.E.P. 706.02 and that the rejection of Claims 41, 45 and 50, and of Claim 42 and 46 which depend from Claims 41 and 45, respectively, is improper and must be withdrawn. Action to this end is requested.

35 U.S.C. 103(a) rejections:

Claims 41-43, 45-47 and 50 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama and/or Park et al. and/or Chen taken with Pintchovski et al. (5, 126, 283). Applicant traverses.

The Examiner states that Koyama and/or Park et al. and/or Chen teach a method for forming a conductive gate of a metal oxide transistor as applied above. Applicant cannot agree. While in response to each of the 102 rejections above, Applicant has shown that each of Koyama, Park et al. and Chen taken alone are deficient with respect to Applicant's Claims 41, 45 and 50, the specific nature of these deficiencies cannot be remedied by any combination of those references.

Both Koyama and Chen lack at least the specific teaching of oxidizing only that portion of the gate adjacent or proximate the gate dielectric or first layer and in fact explicitly teach methods that oxidize all of the sidewalls of gate. Park et al. teaches that sidewall spacers are formed on only that portion of the polysilicon gate portion's sidewalls defined by step "a" (Compare Fig. 4C and Fig. 4E). In Park et al. polysilicon layer 12 has a thickness of between 500-5000 Angstroms (col. 4, line 29). Step "a" is etched to a depth of between 100-1000 Angstroms (*Ibid*, line 50), thus leaving what Applicant computes to be between 400-4000 Angstroms, or as much as 80%, of the polysilicon gate portion that is not covered by a spacer. The subsequent oxidation step of Park et al. therefore will oxidize a substantial portion of gate sidewalls. Thus while Park et al. teaches

protecting a small portion of the gate sidewall, the specific teaching of protecting essentially all of the sidewall so that only the portion of the gate adjacent or proximate the gate dielectric or first layer is oxidized is absent. This result is not improved upon or even substantially changed where Koyama and/or Chen are combined with Park et al. as the oxidation steps of each would result in the oxidation of a substantial portion of the gate sidewalls of Park et al. Thus Koyama and/or Chen and/or Park et al. taken individually or in any combination thereof do not provide or even suggest the teaching alleged by the Examiner.

With regard to Pintchovski et al., the Examiner states that a gate having a polysilicon layer 38, a conductive reaction barrier layer 40 and an overlying metal 42 are taught. However, Pintchovski et al. does not teach or suggest protecting all of the sidewalls of polysilicon layer 38. Since this specific teaching is also lacking from Koyama, Chen and Park et al., no combination of these references with Pintchovski et al. can suggest Applicant's invention as recited in Claims 41, 45 or 50. Applicant respectfully submits, therefore, that the combination of Pintchovski et al. with any combination of Koyama, Chen and Park et al. cannot suggest Applicant's invention as recited in Claims 41, 45 or 50, and is therefore improper and must be withdrawn.. In addition, as Claims 42 and 43 depend from Claim 41, and Claims 46 and 47 depend from Claim 45, the rejection of these dependent claims is also improper and must be withdrawn for at least the reasons stated above for Claims 41 and 45. Action to this end is requested.

Claims 44, 48, 49, 51 and 52 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama and/or Park et al. and/or Chen taken with Pintchovski et al., as applied to claims 41-43, 45-47 and 50 above, and further of Brigham et al. (5, 714, 413) and Kumagai et al. (5, 430, 313). Applicant traverses.

The Examiner alleges that "[a]s previously applied, the relied references teach to form single sidewall barrier spacers on sidewalls of the gate, which teaching is directed to a first embodiment of the present invention ... in which single sidewall barrier spaces are used." In addition, the Examiner states that Brigham et al. and Kumagai et al. are both directed, at least in part, to "forming and using double sidewall spacers" and are thus pertinent to Applicant's second and third embodiments as claimed in Claims 44, 48, 49, 51 and 52, respectively.

Applicant respectfully asserts, however, that even if Brigham et al. and Kumagai et al. were to teach such double sidewall spacers, no combination of the previously cited art teaches or suggests Applicant's underlying invention as recited in independent Claims 41, 45, and 50, from which Claims 44, 48, 49 and 51 depend, respectively, or the invention recited in Claim 52. As the merits of the previously cited art with respect to Claims 41, 45 and 50 is presented extensively above, Applicant refers the Examiner to those arguments and will direct new argument herein only to Claim 52.

Applicant's Claim 52 recites, among other things, covering **all of the sidewalls of the gate structure** and **only oxidizing a portion of the**

**gate structure adjacent the dielectric layer**. (Emphasis added). Applicant has shown above that for each of the other independent claims of the instant application, none of the art cited by the Examiner teaches or suggests these limitations. Therefore Applicant cannot agree that the "relied references teach to form single sidewall barrier spacers on sidewalls of the gate" in the manner of Applicant's claims, and respectfully asserts that these "relied references" are an insufficient basis for this rejection under 35 U.S.C. 103(a), regardless of the teachings of Brigham et al. and/or Kumagai et al. with regard to double sidewall spacers. However, referring to both Brigham et al. and Kumagai et al. it is seen that each reference teaches, in at least one embodiment, oxidation of the entire gate sidewall during the forming of each reference's double sidewall spacer (See, Brigham et al. Figs. 15A-15E and col. 8, line 63 – col. 9, line 23; and Kumagai et al. Figs. 3A-3C and col. 8, line 39 – col. 9, line 40). Hence Brigham et al. and Kumagai et al. cannot remedy the previously shown deficiencies of the relied upon art.

Therefore Applicant respectfully submits that the combination of Brigham et al. and Kumagai et al. with any combination of Koyama, Chen, Park et al. and Pintchovski et al. cannot suggest Applicant's invention as recited in Claims 44, 48, 49, 51 and 52 and is therefore improper and must be withdrawn. Action to this end is requested.

In summary, this application is believed in condition for immediate allowance. Reconsideration and allowance of this application in view of

the amendments and remarks herein is requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, Applicant requests a telephonic interview initiated by the Examiner prior to issuance of any such subsequent Action.

Respectfully submitted,

Dated: 12/14/99

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